



FIG. 1

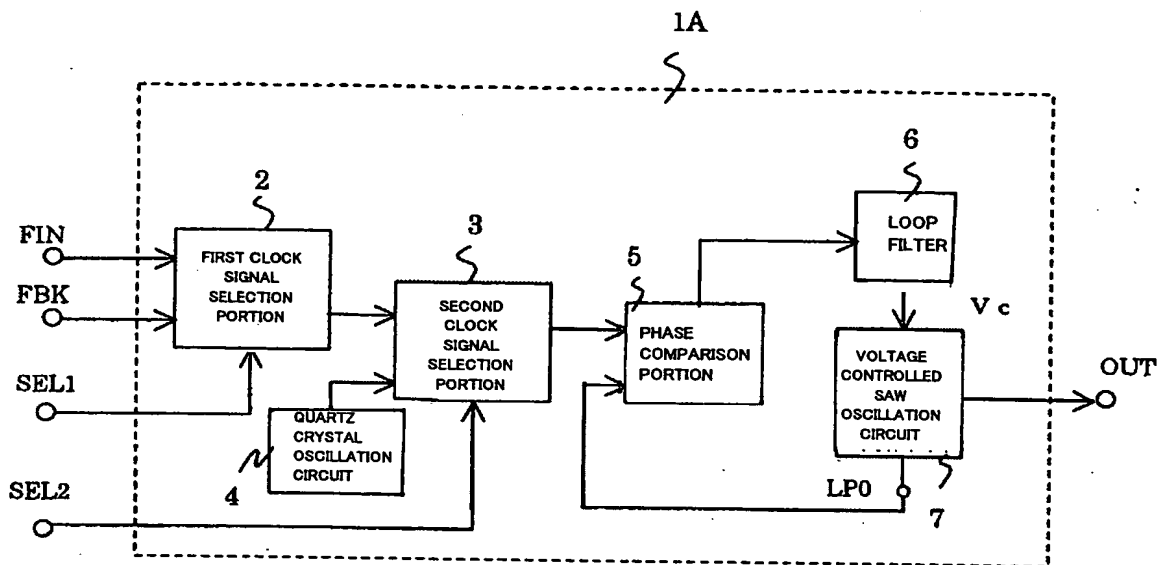
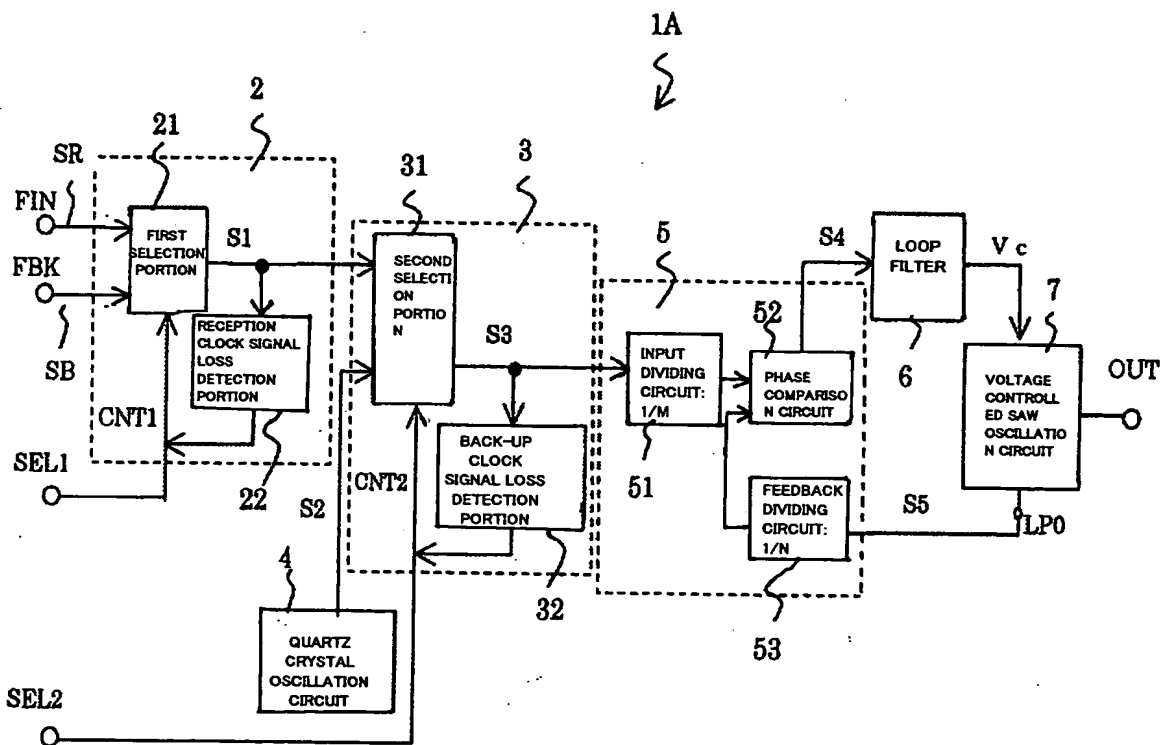
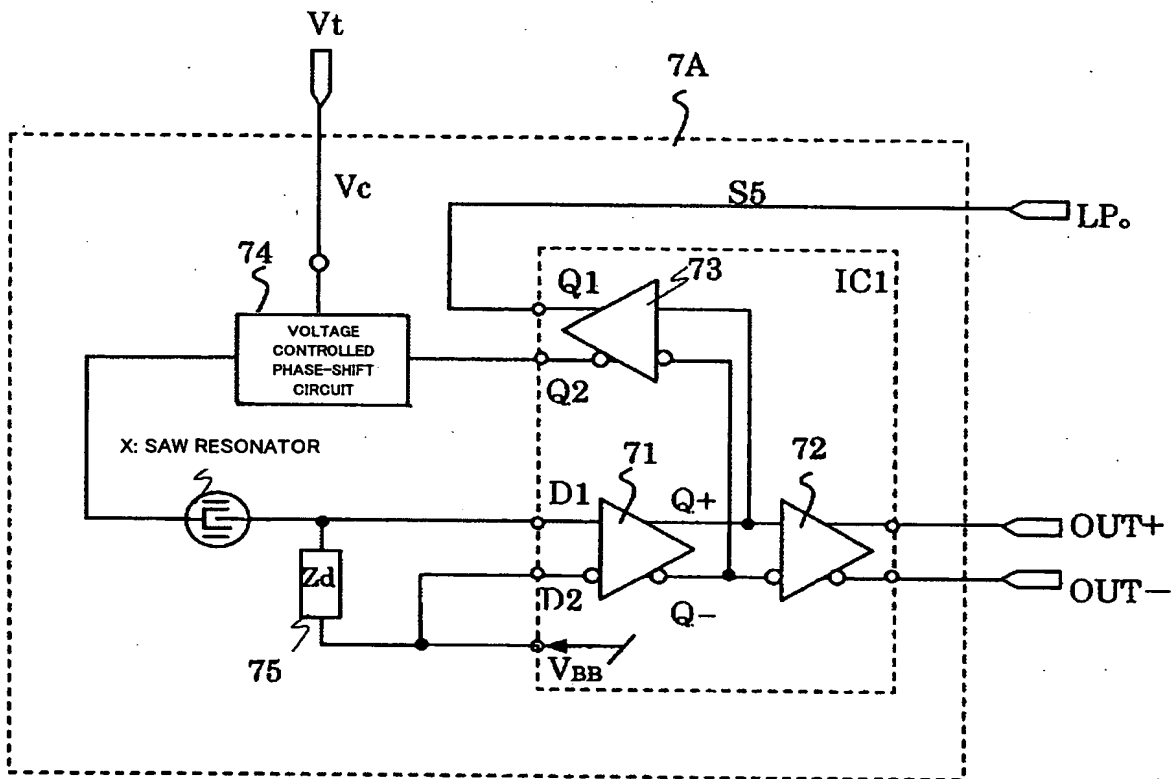


FIG. 2



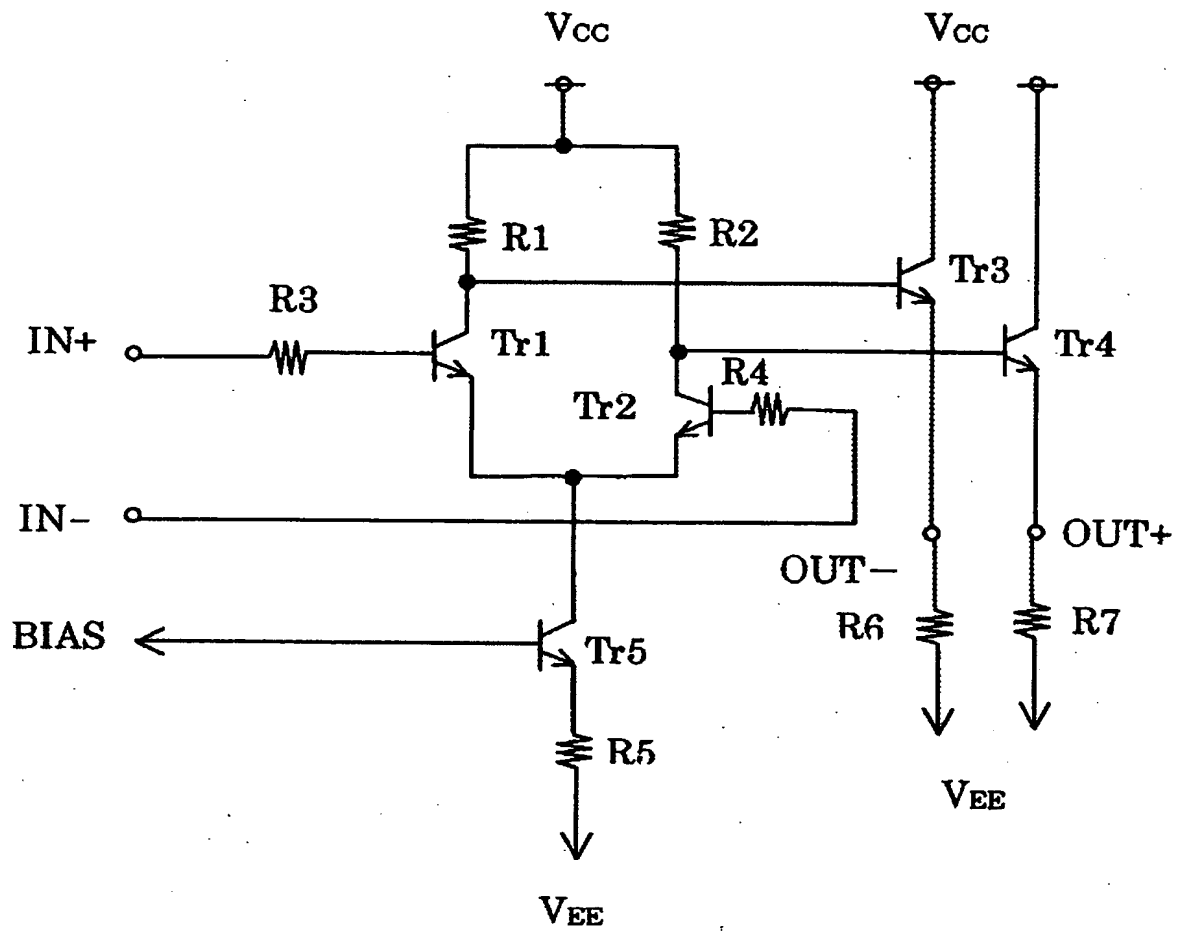
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FIG. 3



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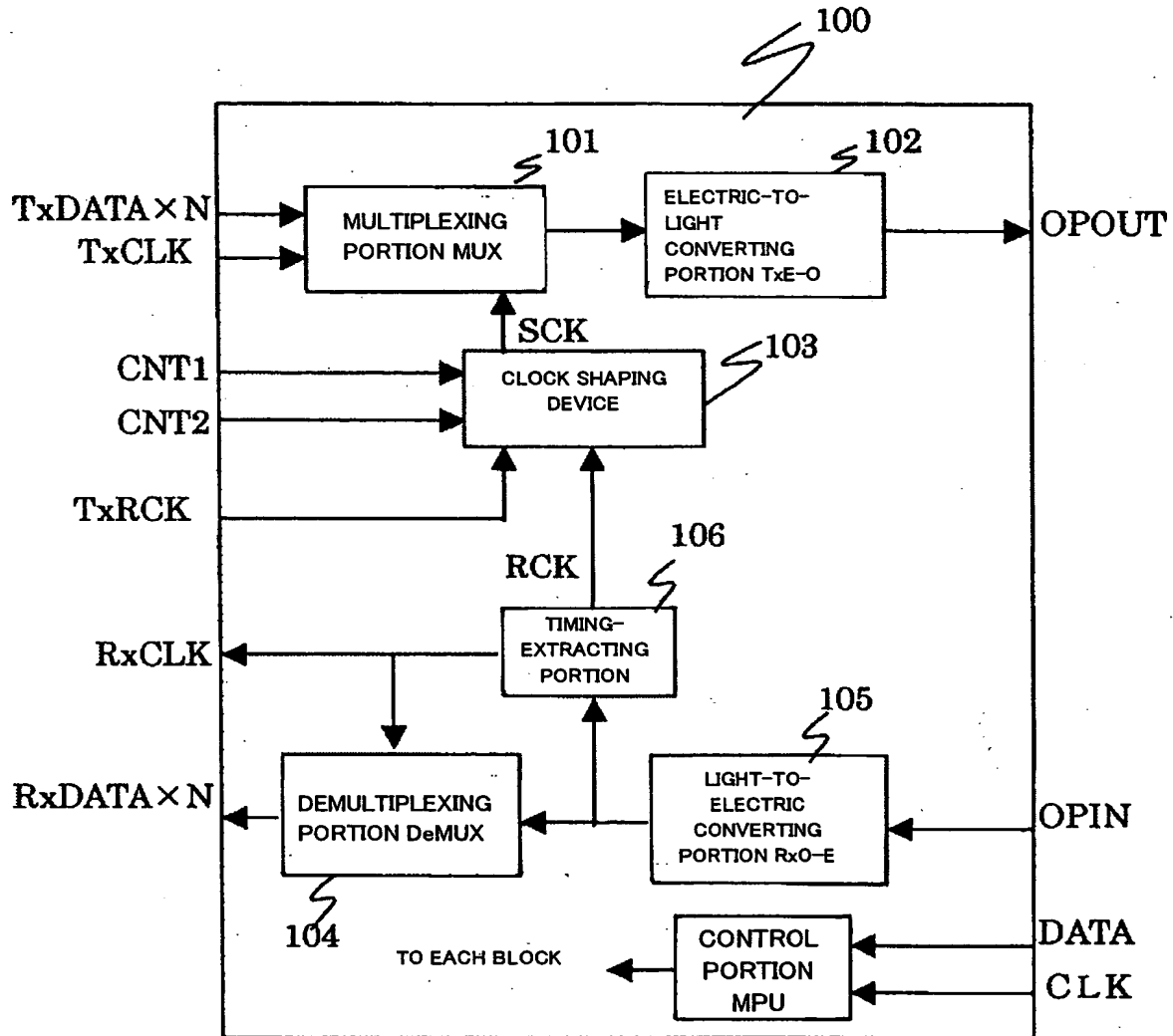
FIG. 4



The diagram illustrates a PLL circuit with a multi-output divider. The main PLL loop includes a first selection portion (21) receiving FIN, FBK, and SB signals, and a reception clock signal loss detection portion (22). A quartz crystal oscillation circuit (4) provides a clock signal to a second selection portion (31) and a back-up clock signal loss detection portion (32). The output of the second selection portion (3) passes through an input dividing circuit (51) with a division ratio of 1/M, then a phase comparison circuit (52), and a feedback dividing circuit (53) with a division ratio of 1/N, before entering a loop filter (6). The output of the loop filter is Vc, which is fed back to the first selection portion (21) and also serves as the control voltage Vc for the divider circuit (7B). The divider circuit (7B) consists of a voltage-controlled phase-shift circuit (74) driven by Vt, which produces signals Q and D. These signals are processed by a multi-output divider IC2 (77) to produce multiple outputs: OUT1, OUT2, ..., OUTn (LPn).

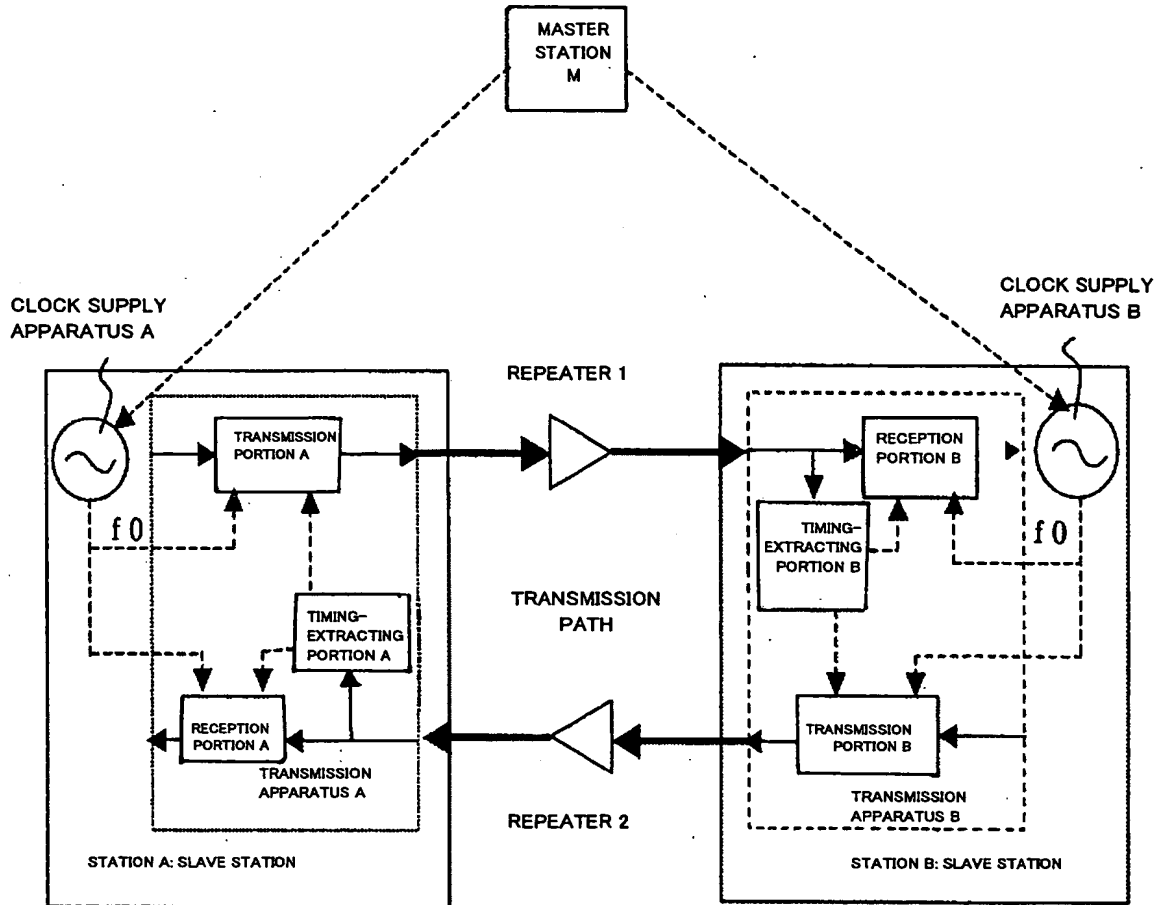
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FIG. 6



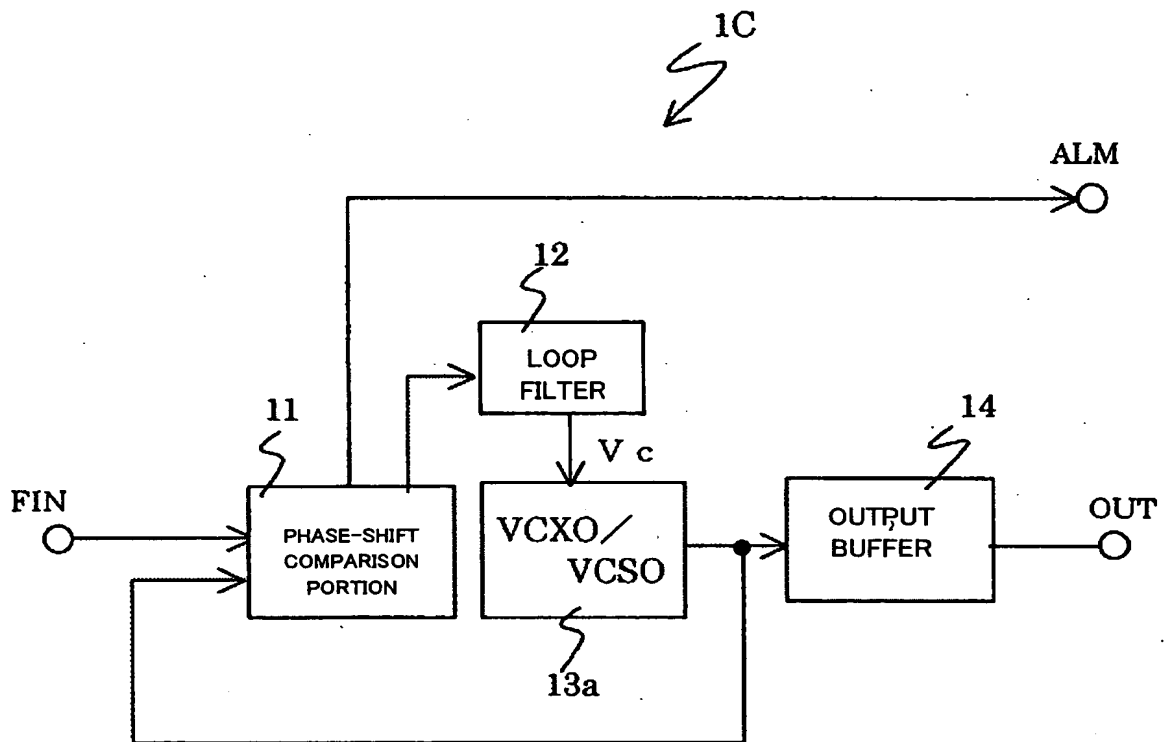
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FIG. 7



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FIG. 8



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FIG. 9

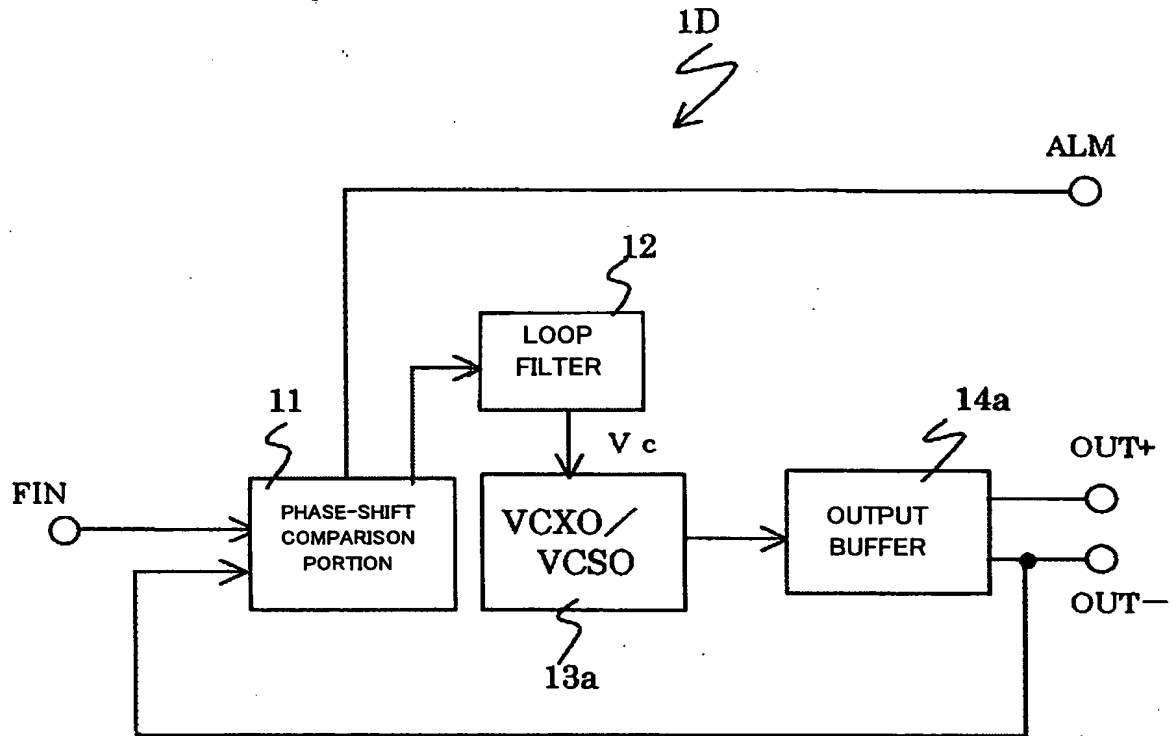


FIG. 10

